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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,719	11/02/2001	Nigel C. Paver	INTL-0650-US (P12391)	3525

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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,719	PAVER, NIGEL C.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been examined.

Papers Received

2. Receipt is acknowledged of application papers submitted, where the papers have been placed of record in the file.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 10 and 38. Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 7-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 7-12 merely manipulate an abstract idea without producing a useful, concrete, and tangible result. The invention of claims 7-12, which comprise a method of generating instructions, does not produce a tangible result since the method does not comprise physical acts and is not performed within a computer. Claim 7 uses the preamble "An article comprising a medium storing instructions that enable a processor-based system." This states that the instructions enable a processor-based system, however, it does not convey that the "article comprising a medium," which is the apparatus to be described based on the scope, enables a processor-based system to do anything. The "article comprising a medium" simply stores the instructions that enable the system. The claim could, for example, read on a book (an article) comprising a page (medium) that contains or stores on it a subroutine of instructions that enable a processor to determine whether a register has been updated; and if the register is updated, set an indicator bit. Thus the claim does not produce a useful, concrete, and tangible result. To expedite a complete examination of the instant application claims 7-12 rejected under 35 USC 101 above are further rejected based on the art as set forth below, where the instructions are in a computer, in anticipation of applicant amending the claims to place them within the four statutory categories of invention. The examiner suggests changing the preamble of claim 7 to read, "An article comprising a medium storing instructions where the article enables a processor-based system to..."

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2-12, 14-17, 21-24, and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 2 mentions the "checking of an indicator bit," however it is unclear as to whether this is the same indicator bit as the parent claim 1 or a different indicator bit. The examiner taking the claim to mean "checking the indicator bit" as shown on page 3, lines 19-20 of the specification and figure 2, which shows a usage indicator that implements the CUP/MUP bits and thus equalizing the terms. Claims 8, 12, 14, and 21 have substantially the same issue and the same interpretation and argument applies. Claims 3-5, 9-11, 15-17, and 22-24 are dependent on these claims and thus inherit the same fault.

9. Claim 6 uses the phrase "assigning a single indicator bit to a plurality of registers," but it is unknown whether this single indicator bit is the indicator bit of the independent parent claim or a different indicator bit. The examiner is taking the claim to mean "assigning as the indicator bit a single indicator bit..." and interpreting the Applicant to mean to show the use of a single bit instead of the possibility of a bit among a plurality of bits due to the open language of the parent claim. Claim 27 has substantially the same issue and the same interpretation and argument applies.

10. Claim 7 uses the preamble "An article comprises a medium storing instructions that enable a processor-based system to..." but it is unclear as to whether the article or instructions are enabling the processor-based system. The examiner is taking the claim to mean, "An article comprising a medium storing instructions, where the medium enables a processor-based system to..." so that the claim becomes statutory under 35 USC §101.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-4, 6-10, 12-16, 18-23, and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Hankins (4,233,601).

13. In regard to claim 1, Hankins discloses a method comprising:

a. determining whether a register has been updated;

b. and if the register is updated, setting an indicator bit.

Column 7, lines 5-19 shows that it is determined if a register 30-32 has been updated, more specifically if data has been shifted into or out of the register. An indicator is used to show this and the indicator is updated accordingly.

14. In regard to claim 2, Hankins discloses the method of claim 1 including determining whether the register has been updated by checking the indicator bit.

Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read or not.

15. In regard to claim 3, Hankins discloses the method of claim 2 wherein if the register has not been updated, refraining from transferring the contents of the register back to a memory. Column 6, lines 29-31 show that a read access of the registers 30-32 output the contents to registers (a memory) 33 to 35.Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read if the data has been shifted in the registers, that is the registers were updated. Therefore, if the registers haven't been updated, the read will not take place.

16. In regard to claim 4, Hankins discloses the method of claim 2 including determining whether the register has been updated and if so, saving the contents of the register to memory. Column 6, lines 29-31 show that a read access of the registers 30-32 output the contents to registers (a memory) 33 to 35.Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read if the data has been shifted in the registers, that is the registers were updated. When the update has a occurred, the next read happens and the contents are saved into memory (registers 33-35).

17. In regard to claim 6, Hankins discloses the method of claim 1 including assigning the indicator bit as a single indicator bit to a plurality of registers. Column 7, lines 7-9 show that a single (one) bistable is used as an indicator for the plurality of registers 30-32. The included IEEE definition of bistable is a

device that is capable of assuming one of two states, and thus is a device that stores a single bit, which indicates one of two states, 0 or 1.

18. In regard to claim 7, Hankins discloses an article comprising a medium storing instructions where the article enables a processor-based system to: determine whether a register has been updated; and if the register is updated, set an indicator bit. Column 7, lines 5-19 shows that it is determined if a register 30-32 has been updated, more specifically if data has been shifted into or out of the register. An indicator is used to show this and the indicator is updated accordingly. Column 5, lines 22-28 show that a processor loads the store and since the included IEEE definition of processor shows that a processor interprets and executes instructions, the processor must be enabled to perform the above functionality based on these inherently stored instructions.

19. In regard to claim 8, Hankins discloses the article of claim 7 further storing instructions that enable the processor-based system to determine whether the register has been updated by checking the indicator bit. Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read or not.

20. In regard to claim 9, Hankins discloses the article of claim 8 further storing instructions that enable the processor-based system to refrain from transferring the contents of the register back to a memory if the register has not been updated. Column 6, lines 29-31 show that a read access of the registers 30-32 output the contents to registers (a memory) 33 to 35.Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read if the

data has been shifted in the registers, that is the registers were updated. Therefore, if the registers haven't been updated, the read will not take place.

21. In regard to claim 10, Hankins discloses the article of claim 8 further storing instructions that enable the processor-based system to determine whether the register has been updated and if so, save the contents of the register to memory. Column 6, lines 29-31 show that a read access of the registers 30-32 output the contents to registers (a memory) 33 to 35. Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read if the data has been shifted in the registers, that is the registers were updated. When the update has occurred, the next read happens and the contents are saved into memory (registers 33-35).

22. In regard to claim 12, Hankins discloses the article of claim 10 further storing instructions that enable the processor-based system to save the contents of a plurality of registers to memory if the indicator bit is set, as described above. As shown above, registers are saved to memory when an indicator signifying an update is set. Column 7, lines 17-19 show that the register 30-32 are always used simultaneously and thus a plurality of registers are read and saved.

23. In regard to claim 13, Hankins discloses a processor comprising:

a. a register (column 7, lines 7-19, registers 30-32 of figure 5);

b. and a storage storing instructions to determine whether a register has been updated and if the register is updated, set an indicator bit. Column 7, lines 5-19 shows that it is determined if a register 30-32 has been updated, more specifically if data has been shifted into or out of the

register. An indicator is used to show this and the indicator is updated accordingly. Column 5, lines 22-28 show that a processor loads the store and since the included IEEE definition of processor shows that a processor interprets and executes instructions, the processor must be enabled to perform the above functionality based on these inherently stored instructions.

24. In regard to claim 14, Hankins discloses the processor of claim 13 wherein said storage stores instructions that enable the processor to determine whether the register has been updated by checking the indicator bit. Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read or not.

25. In regard to claim 15, Hankins discloses the processor of claim 14 wherein said storage stores instructions that enable the processor to refrain from transferring the contents of the register back to a memory. Column 6, lines 29-31 show that a read access of the registers 30-32 output the contents to registers (a memory) 33 to 35. Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read if the data has been shifted in the registers, that is the registers were updated. Therefore, if the registers haven't been updated, the read will not take place.

26. In regard to claim 16, Hankins discloses the processor of claim 14 wherein said storage stores instructions that enable the processor to determine whether the register has been updated and if so, save the contents of the register to memory. Column 6, lines 29-31 show that a read access of the registers 30-32

output the contents to registers (a memory) 33 to 35. Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read if the data has been shifted in the registers, that is the registers were updated. When the update has occurred, the next read happens and the contents are saved into memory (registers 33-35).

27. In regard to claim 18, Hankins discloses the processor of claim 13 including a storage to store said bit. Column 7, lines 7-9 show that a single (one) bistable is used as an indicator for the plurality of registers 30-32. The included IEEE definition of bistable is a device that is capable of assuming one of two states, and thus is a device that stores a single bit, which indicates one of two states, 0 or 1.

28. In regard to claim 19, Hankins discloses a system comprising: a processor; a register coupled to said processor; and a storage storing instructions to determine whether a register has been updated and if the register is updated, set the indicator bit. Column 7, lines 5-19 shows that it is determined if a register 30-32 has been updated, more specifically if data has been shifted into or out of the register. An indicator is used to show this and the indicator is updated accordingly. Column 5, lines 22-28 show that a processor loads the store and since the included IEEE definition of processor shows that a processor interprets and executes instructions, the processor must be enabled to perform the above functionality based on these inherently stored instructions.

29. In regard to claim 20, Hankins discloses the system of claim 19 including a memory and an interface between said memory and said processor. Figure 5

shows a memory in registers 33-35 and illustrates an interface coupling the registers 30-32 with this memory.

30. In regard to claim 21, Hankins discloses the system of claim 20 wherein said storage stores instructions that enable the processor to determine whether the register has been updated by checking the indicator bit. Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read or not.

31. In regard to claim 22, Hankins discloses the system of claim 21 wherein said storage stores instructions that enable the processor to refrain from transferring the contents of the register back to the memory. Column 6, lines 29-31 show that a read access of the registers 30-32 output the contents to registers (a memory) 33 to 35. Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read if the data has been shifted in the registers, that is the registers were updated. Therefore, if the registers haven't been updated, the read will not take place.

32. In regard to claim 23, Hankins discloses the system of claim 21 wherein said storage stores instructions that enable the processor to determine whether the register has been updated and if so, save the contents of the register to the memory. Column 6, lines 29-31 show that a read access of the registers 30-32 output the contents to registers (a memory) 33 to 35. Column 7, lines 17-19 show that the indicator is checked so as to know whether to initiate the next read if the data has been shifted in the registers, that is the registers were updated.

When the update has occurred, the next read happens and the contents are saved into memory (registers 33-35).

33. In regard to claim 25, Hankins discloses the system of claim 19 including a storage to store said bit. Column 7, lines 7-9 show that a single (one) bistable is used as an indicator for the plurality of registers 30-32. The included IEEE definition of bistable is a device that is capable of assuming one of two states, and thus is a device that stores a single bit, which indicates one of two states, 0 or 1.

34. In regard to claim 26, Hankins discloses the system of claim 19 including a control register storing said bit and wherein said storage storing instructions and control register are part of said processor. Column 7, lines 7-9 show that a single (one) bistable is used as an indicator for the plurality of registers 30-32. The included IEEE definition of bistable is a device that is capable of assuming one of two states, and thus is a device that stores a bit, which indicates one of two states, 0 or 1. The included IEEE definition of register simply shows that it is a device capable of retaining information and thus the bistable is a register. Since the stored indicator bit specifies whether to update a memory or not, it controls this behavior and an appropriate name for the register is a control register.

35. In regard to claim 27, Hankins discloses the system of claim 19 including a plurality of registers coupled to said processor and the indicator bit being a single indicator bit for all of those registers. Column 7, lines 7-9 show that a single (one) bistable is used as an indicator for the plurality of registers 30-32. The included IEEE definition of bistable is a device that is capable of assuming one of two

states, and thus is a device that stores a single bit, which indicates one of two states, 0 or 1.

Claim Rejections - 35 USC § 103

36. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

37. Claims 5, 11, 17, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hankins in view of Nikhil (*T: A Multithreaded Massively Parallel Architecture) and Hennessy (Computer architecture A Quantitative Approach).

38. In regard to claim 5,

a. Hankins discloses the method of claim 4.

b. Hankins does not disclose including saving the register contents to memory on a context change or having multiple contexts at all.

c. Nikhil has taught the use of a multithreaded processor that switches threads or contexts as detailed in Section 3.2. The first column of page 161 shows that a context is equivalent to a frame pointer. Section 4.1 shows on page 162 that no implicit saving of registers is done and thus no assumptions can be made about register contents when switching contexts. The registers are volatile or ephemeral across contexts or threads and thus must be saved (to some memory) explicitly upon

switching. This is shown in the first column of page 160 where it is shown that any change in context requires saving, though the disclosure prefers not to save state for Interrupts, it still must occur for switches due to a load request as shown in section 3.2

d. Nikhil has shown in the introduction that the disclosed multithreaded processor is massively parallel processor and thus many operations are completed in parallel, which increases performance since more work is done at one time. Pages 438-439 of Hennessy have shown that saving the state or all the current information (including registers) of a process or context to disk (memory) is the safest way to switch contexts. This ability to increase parallelism for increased performance with multithreading and to save the registers when switching threads or contexts in order to have the most safe execution would have motivated one of ordinary skill in the art to modify the design of Hankins to implement the multithreaded design of Nikhil.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Hankins to implement the multithreaded design of Nikhil so that performance may be increased through parallelism and context switches may be as safe as possible.

39. In regard to claim 11,

a. Hankins discloses the article of claim 10.

b. Hankins does not disclose further storing instructions that enable the processor-based system to save the register contents to memory on a context change or having multiple contexts at all.

c. Nikhil has taught the use of a multithreaded processor that switches threads or contexts as detailed in Section 3.2. The first column of page 161 shows that a context is equivalent to a frame pointer. Section 4.1 shows on page 162 that no implicit saving of registers is done and thus no assumptions can be made about register contents when switching contexts. The registers are volatile or ephemeral across contexts or threads and thus must be saved (to some memory) explicitly upon switching. This is shown in the first column of page 160 where it is shown that any change in context requires saving, though the disclosure prefers not to save state for Interrupts, it still must occur for switches due to a load request as shown in section 3.2

d. Nikhil has shown in the introduction that the disclosed multithreaded processor is massively parallel processor and thus many operations are completed in parallel, which increases performance since more work is done at one time. Pages 438-439 of Hennessy have shown that saving the state or all the current information (including registers) of a process or context to disk (memory) is the safest way to switch contexts. This ability to increase parallelism for increased performance with multithreading and to save the registers when switching threads or contexts in order to have the most safe execution would have motivated

one of ordinary skill in the art to modify the design of Hankins to implement the multithreaded design of Nikhil.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Hankins to implement the multithreaded design of Nikhil so that performance may be increased through parallelism and context switches may be as safe as possible.

40. In regard to claim 17,

a. Hankins discloses the article of claim 16.

b. Hankins does not disclose wherein said storage stores instructions that enable the processor to save the register contents to memory on a context change or having multiple contexts at all.

c. Nikhil has taught the use of a multithreaded processor that switches threads or contexts as detailed in Section 3.2. The first column of page 161 shows that a context is equivalent to a frame pointer. Section 4.1 shows on page 162 that no implicit saving of registers is done and thus no assumptions can be made about register contents when switching contexts. The registers are volatile or ephemeral across contexts or threads and thus must be saved (to some memory) explicitly upon switching. This is shown in the first column of page 160 where it is shown that any change in context requires saving, though the disclosure prefers not to save state for Interrupts, it still must occur for switches due to a load request as shown in section 3.2

d. Nikhil has shown in the introduction that the disclosed multithreaded processor is massively parallel processor and thus many operations are completed in parallel, which increases performance since more work is done at one time. Pages 438-439 of Hennessy have shown that saving the state or all the current information (including registers) of a process or context to disk (memory) is the safest way to switch contexts. This ability to increase parallelism for increased performance with multithreading and to save the registers when switching threads or contexts in order to have the most safe execution would have motivated one of ordinary skill in the art to modify the design of Hankins to implement the multithreaded design of Nikhil.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Hankins to implement the multithreaded design of Nikhil so that performance may be increased through parallelism and context switches may be as safe as possible.

41. In regard to claim 24,

a. Hankins discloses the article of claim 23.

b. Hankins does not disclose wherein said storage stores instructions that enable the processor to save the register contents to memory on a context change or having multiple contexts at all.

c. Nikhil has taught the use of a multithreaded processor that switches threads or contexts as detailed in Section 3.2. The first column of page 161 shows that a context is equivalent to a frame pointer. Section 4.1

shows on page 162 that no implicit saving of registers is done and thus no assumptions can be made about register contents when switching contexts. The registers are volatile or ephemeral across contexts or threads and thus must be saved (to some memory) explicitly upon switching. This is shown in the first column of page 160 where it is shown that any change in context requires saving, though the disclosure prefers not to save state for Interrupts, it still must occur for switches due to a load request as shown in section 3.2

d. Nikhil has shown in the introduction that the disclosed multithreaded processor is massively parallel processor and thus many operations are completed in parallel, which increases performance since more work is done at one time. Pages 438-439 of Hennessy have shown that saving the state or all the current information (including registers) of a process or context to disk (memory) is the safest way to switch contexts. This ability to increase parallelism for increased performance with multithreading and to save the registers when switching threads or contexts in order to have the most safe execution would have motivated one of ordinary skill in the art to modify the design of Hankins to implement the multithreaded design of Nikhil.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Hankins to implement the multithreaded design of Nikhil so that performance may be increased through parallelism and context switches may be as safe as possible.

Conclusion

42. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

43. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references have been cited to further show the art with respect to register update indicators.

US Pat No 5,926,646 to Pickett shows indicating updating an MSR register by the operations it then controls.

US Pat No 5,859,999 to Morris discloses a mask used to indicate registers to update.

US Pat No 5,597,971 to Saito teaches using an LED indicator on an update of a register.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
June 24, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100